AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, comprising:

a level shift core circuit which is controlled by a control circuit, wherein:

the level shift core circuit, being fed from the second power supply, receives level shift input signals output from the first logic circuit and control signals output from the control circuit and outputs level shift output signals to be input to the second logic circuit; the control circuit comprises: a first NOR circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; and a second NOR circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; where the control circuit outputs the output signals of the first and second NOR circuits as control signals to the level shift core circuit; and

the level shift core circuit comprises: a PMOS cross-coupled latch including a first plurality of PMOSs, a differential PMOS switch including a second plurality of PMOSs, and a differential NMOS switch including a plurality of NMOSs:

wherein each PMOS of the second plurality of PMOSs has a source connected to a drain of a PMOS of the first plurality of PMOSs, a drain connected to the level shift output, and a gate connected to one of the control signals from the control circuit;

wherein each PMOS of the first plurality of PMOSs has a source connected to the second power supply, a gate connected to the level shift output through the drain of another PMOS of the second plurality of PMOSs, where the other PMOS of the second plurality PMOSs does not share a drain to source connection with the PMOS of the first plurality of PMOSs; and

wherein each NMOS of the differential NMOS switch has a source connected to the ground voltage GND, a drain connected to the level shift output, and a gate connected to the level shift input.

2. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, comprising:

a level shift core circuit which is controlled by a control circuit, wherein:

the level shift core circuit, being fed from the second power supply, receives level shift input signals output from the first logic circuit and control signals output from the control circuit and outputs level shift output signals to be input to the second logic circuit;

the control circuit comprises: a first NOR circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; a second NOR circuit fed from the second power supply, which

receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; and a plurality of inverters fed from the second power supply, which receives the outputs of the NOR circuits, respectively; where the control circuit outputs the output signals of the respective first and second NOR circuits and the inverters as control signals to the level shift core circuit; and the level shift core circuit comprises: a PMOS cross-coupled latch including a first plurality of PMOSs, a differential PMOS switch including a second plurality of PMOSs, and a differential NMOS switch including a plurality of NMOSs:

wherein each PMOS of the second plurality of PMOSs has a source connected to a drain of a PMOS of the first plurality of PMOSs, a drain connected to the level shift output, and a gate connected to one of the control signals from the control circuit;

wherein each PMOS of the first plurality of PMOSs has a source connected to the second power supply, a gate connected to the level shift output through the drain of another PMOS of the second plurality of PMOSs, where the other PMOS of the second plurality PMOSs does not share a drain to source connection with the PMOS of the first plurality of PMOSs; and

wherein each NMOS of the differential NMOS switch has a source connected to the ground voltage GND, a drain connected to the level shift output, and a gate connected to the level shift input.

3. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, comprising:

a level shift core circuit for implementing a level shift;

a pull-up and pull-down circuit fed from the second power supply for pulling up and/ or pulling down level shift output signals from the level shift core circuit; and

a control circuit fed from the second power supply, which receives level shift input signals output from the first logic circuit and the level shift output signals for controlling the pull-up and pull-down circuit, wherein:

the control circuit comprises: a first NOR circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; and a second NOR circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals;

the control circuit outputs the output signals of the first and second NOR circuits as control signals; and

the level shift core circuit comprises: a PMOS cross-coupled latch including a first plurality of PMOSs, a differential PMOS switch including a second plurality of PMOSs, and a differential NMOS switch including a plurality of NMOSs:

wherein each PMOS of the second plurality of PMOSs has a source connected to a drain of a PMOS of the first plurality of PMOSs, a drain connected to the level shift output, and a gate connected to one of the control signals from the control circuit;

wherein each PMOS of the first plurality of PMOSs has a source connected to the second power supply, a gate connected to the level shift output through the drain of another PMOS of

the second plurality of PMOSs, where the other PMOS of the second plurality PMOSs does not share a drain to source connection with the PMOS of the first plurality of PMOSs; and

wherein each NMOS of the differential NMOS switch has a source connected to the ground voltage GND, a drain connected to the level shift output, and a gate connected to the level shift input.

4. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, comprising:

a level shift core circuit for implementing a level shift;

a pull-up and pull-down circuit fed from the second power supply for pulling up and/ or pulling down level shift output signals from the level shift core circuit; and

a control circuit fed from the second power supply, which receives level shift input signals output from the first logic circuit and the level shift output signals for controlling the pull-up and pull-down circuit, wherein:

the control circuit comprises: a first NOR circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; a second NOR circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; and a plurality of inverters fed from the second power supply, which receives the outputs of the NOR circuits, respectively;

the control circuit outputs the output signals of the respective first and second NOR circuits and the inverters as control signals; and

the level shift core circuit comprises: a PMOS cross-coupled latch including a first plurality of PMOSs, a differential PMOS switch including a second plurality of PMOSs, and a differential NMOS switch including a plurality of NMOSs:

wherein each PMOS of the second plurality of PMOSs has a source connected to a drain of a PMOS of the first plurality of PMOSs, a drain connected to the level shift output, and a gate connected to one of the control signals from the control circuit;

wherein each PMOS of the first plurality of PMOSs has a source connected to the second power supply, a gate connected to the level shift output through the drain of another PMOS of the second plurality of PMOSs, where the other PMOS of the second plurality PMOSs does not share a drain to source connection with the PMOS of the first plurality of PMOSs; and

wherein each NMOS of the differential NMOS switch has a source connected to the ground voltage GND, a drain connected to the level shift output, and a gate connected to the level shift input.

5. (previously presented): The level shift circuit claimed in one of claims 1 to 4, wherein the NOR circuit has CMOS circuitry, and each PMOS connected to the level shift input signal is a transistor which satisfies at least one of the conditions that the channel width/ channel length ratio is low or that the polarity of the threshold voltage is negative and the absolute value of the threshold voltage is large.

6. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, comprising:

a level shift core circuit which is controlled by a control circuit, wherein:

the level shift core circuit, being fed from the second power supply, receives level shift input signals output from the first logic circuit and control signals output from the control circuit and outputs level shift output signals to be input to the second logic circuit;

the control circuit comprises: a first NAND circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; and a second NAND circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; where the control circuit outputs the output signals of the first and second NAND circuits as control signals to the level shift core circuit; and

the level shift core circuit comprises: a PMOS cross-coupled latch including a first plurality of PMOSs, a differential PMOS switch including a second plurality of PMOSs, and a differential NMOS switch including a plurality of NMOSs:

wherein each PMOS of the second plurality of PMOSs has a source connected to a drain of a PMOS of the first plurality of PMOSs, a drain connected to the level shift output, and a gate connected to one of the control signals from the control circuit;

wherein each PMOS of the first plurality of PMOSs has a source connected to the second power supply, a gate connected to the level shift output through the drain of another PMOS of

the second plurality of PMOSs, where the other PMOS of the second plurality PMOSs does not share a drain to source connection with the PMOS of the first plurality of PMOSs; and

wherein each NMOS of the differential NMOS switch has a source connected to the ground voltage GND, a drain connected to the level shift output, and a gate connected to the level shift input.

7. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, comprising:

a level shift core circuit for implementing a level shift;

a pull-up and pull-down circuit fed from the second power supply for pulling up and/ or pulling down level shift output signals from the level shift core circuit; and

a control circuit fed from the second power supply, which receives level shift input signals output from the first logic circuit and the level shift output signals for controlling the pull-up and pull-down circuit, wherein:

the control circuit comprises: a first NAND circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; and a second NAND circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals;

the control circuit outputs the output signals of the first and second NAND circuits as control signals; and

the level shift core circuit comprises: a PMOS cross-coupled latch including a first plurality of PMOSs, a differential PMOS switch including a second plurality of PMOSs, and a differential NMOS switch including a plurality of NMOSs:

wherein each PMOS of the second plurality of PMOSs has a source connected to a drain of a PMOS of the first plurality of PMOSs, a drain connected to the level shift output, and a gate connected to one of the control signals from the control circuit;

wherein each PMOS of the first plurality of PMOSs has a source connected to the second power supply, a gate connected to the level shift output through the drain of another PMOS of the second plurality of PMOSs, where the other PMOS of the second plurality PMOSs does not share a drain to source connection with the PMOS of the first plurality of PMOSs; and

wherein each NMOS of the differential NMOS switch has a source connected to the ground voltage GND, a drain connected to the level shift output, and a gate connected to the level shift input.

8. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, comprising:

a level shift core circuit for implementing a level shift;

a pull-up and pull-down circuit fed from the second power supply for pulling up and/ or pulling down level shift output signals from the level shift core circuit; and

a control circuit fed from the second power supply, which receives level shift input signals output from the first logic circuit and the level shift output signals for controlling the pull-up and pull-down circuit, wherein:

the control circuit comprises: a first NAND circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; a second NAND circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; and a plurality of inverters fed from the second power supply, which receives the outputs of the first and second NAND circuits, respectively;

the control circuit outputs the output signals of the respective first and second NAND circuits and the inverters as control signals; and

the level shift core circuit comprises: a PMOS cross-coupled latch including a first plurality of PMOSs, a differential PMOS switch including a second plurality of PMOSs, and a differential NMOS switch including a plurality of NMOSs:

wherein each PMOS of the second plurality of PMOSs has a source connected to a drain of a PMOS of the first plurality of PMOSs, a drain connected to the level shift output, and a gate connected to one of the control signals from the control circuit;

wherein each PMOS of the first plurality of PMOSs has a source connected to the second power supply, a gate connected to the level shift output through the drain of another PMOS of the second plurality of PMOSs, where the other PMOS of the second plurality PMOSs does not share a drain to source connection with the PMOS of the first plurality of PMOSs; and

wherein each NMOS of the differential NMOS switch has a source connected to the ground voltage GND, a drain connected to the level shift output, and a gate connected to the level shift input.

9. (previously presented): The level shift circuit claimed in one of claims 6, 7, 8, or 14, wherein the NAND circuit has CMOS circuitry, and each PMOS connected to the level shift input signal is a transistor which satisfies at least one of the conditions that the channel width/ channel length ratio is low or that the polarity of the threshold voltage is negative and the absolute value of the threshold voltage is large.

10. (canceled).

11. (previously presented): The level shift circuit claimed in one of claims 3, 4, 7, or 8, wherein the pull-up and pull-down circuit comprises: a plurality of PMOSs each having a source connected to the second power supply, a gate connected to one of the control signals from the control circuit, and a drain connected to the level shift output; and a plurality of NMOSs each having a source connected to the ground voltage GND, a gate connected to one of the control signals from the control circuit, and a drain connected to the level shift output.

12. (canceled).

13. (canceled).

14. (previously presented): A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, comprising:

a level shift core circuit which is controlled by a control circuit, wherein:

the level shift core circuit, being fed from the second power supply, receives level shift input signals output from the first logic circuit and control signals output from the control circuit and outputs level shift output signals to be input to the second logic circuit;

the control circuit comprising: a first NAND circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; a second NAND circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; and a plurality of inverters fed from the second power supply, which receives the outputs of the NAND circuits, respectively; where the control circuit outputs the output signals of the respective first and second NAND circuits and the inverters as control signals to the level shift core circuit, and

the level shift core circuit comprises: a PMOS cross-coupled latch including a first plurality of PMOSs, a differential PMOS switch including a second plurality of PMOSs, and a differential NMOS switch including a plurality of NMOSs:

wherein each PMOS of the second plurality of PMOSs has a source connected to a drain of a PMOS of the first plurality of PMOSs, a drain connected to the level shift output, and a gate connected to one of the control signals from the control circuit;

wherein each PMOS of the first plurality of PMOSs has a source connected to the second power supply, a gate connected to the level shift output through the drain of another PMOS of the second plurality of PMOSs, where the other PMOS of the second plurality PMOSs does not share a drain to source connection with the PMOS of the first plurality of PMOSs; and

wherein each NMOS of the differential NMOS switch has a source connected to the ground voltage GND, a drain connected to the level shift output, and a gate connected to the level shift input.

15. (previously presented): The level shift circuit claimed in one of claims 1, 2, 6, or 14, further comprising: a pull up and pull down circuit having a pull up circuit and a pull down circuit which pulls up and/or pulls down the level shift output signals, wherein the control circuit is configured to output control signals to the pull up and pull down circuit for controlling at least one of the pull up circuit and the pull down circuit.

16. (previously presented): The level shift circuit of claim 15, wherein the pull-up circuit comprises: a plurality of PMOSs each having a source connected to the second power supply, a gate connected to one of the control signals from the control circuit, and a drain connected to the level shift output; and

the pull-down circuit comprises: a plurality of NMOSs each having a source connected to the ground voltage GND, a gate connected to a control signal from the control circuit, and a drain connected to the level shift output.

17. - 21. (canceled).